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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/754,483	CONLEY ET AL.	
	Examiner	Art Unit	
	Yaima Campos	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. As per the instant Application having Application number 10/754,483, the examiner acknowledges the applicant's submission of the amendment dated October 24, 1007. At this point, claims 1, 5, 13, and 19 have been amended and claims 26-35 have been canceled. Claims 1-25 are pending.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 24, 2007 has been entered.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 1-25** are rejected under 35 U.S.C. 103(a) as being unpatentable over Suda (US 2004/0123059) in view of Kim et al. (US 2004/0123059).

5. As per **claim 1**, Suda discloses "A method for reading data from a memory card that provides non-volatile data storage, *defined by a contiguous range of addresses*" as **["the present invention relates to a memory card authentication system, a memory card host device, a memory card, a storage area switching method, and a storage area switching program, which are capable of switching plural storage areas" (Page 1, paragraph 0003) address space within memory card 3 (See Figure 1) and (Figure 5)]**

"said method comprising: (a) accessing volume information stored in a *range of addresses that is a proper subset of the contiguous range of addresses that defines the address space*; **["It is possible to allow the memory card host device 1 to execute a procedure for reading out internal register values of the memory card and a procedure for judging whether or not the memory card has plural storage areas by mean of reading out the storage switching program form the program storage device" (Page 2, Paragraph 0027) and "at least one internal register 12a with a flag indicating the quantity of the storage areas added to a reserved area thereof" (Page 2, Paragraph 0028)]**. Applicant should note that as the "internal register 18" stores the number of areas inside a memory card, this number of areas corresponds to the claimed "volume information." The number of areas inside a memory card represents the number of volumes inside a memory card, and therefore, represents "volume information." Furthermore, Suda discloses **[*"FIG. 1 shows the conventional memory card, in which flags are added to convention reserved areas. Each of the internal registers 12a, 12b, 12c, and 12d of the memory card 3 includes first to third bit string 20a, 20b, and 20c... The first bit string 20a equivalent to the first 23 bits of the internal register indicates a characteristic of the memory card... The second bit string 20b equivalent to the first 23 bits of the internal register indicates*

***a characteristic of the memory card 3... The third bit string 20c equivalent to 4 bits subsequent to the second bit string is also a convention reserved area of the internal register... Information indicating the quantity of storage areas is added hereto... In the memory card 3, shown in FIG. 1, a flag indicating 4 is et to each of the third bit strings of the internal register... when the memory card 3 has four storage areas*" (Par. 0039; See Figure 1 and related text)].** Applicant should note that Examiner interprets the "first storage areas 11a-12a, 11b-12b, 11c-12c and 11d-12d" as a continuous address space which is shown as bit strings comprising fields 20a, 20b and 20c. Therefore, as Suda stores volume information indicating the number of storage areas within field 20c of internal registers, which are shown to comprise a range of address that is a "proper subset" (*which comprises a relative term, as any subset within a storage address space can be considered a proper subset*) of a contiguous range of addresses, Suda discloses "accessing volume information stored in a *range of addresses that is a proper subset of the contiguous range of addresses that defines the address space*." Applicant should further note that Suda expressly discloses **["FIG. 5 shows the memory card 3 in which the plural storage areas 11a, 11b, and 11c severally include the internal registers 12a, 12b, and 12c" (Figure 5 and related text) wherein contiguous address space comprising addresses 00000-xFFFF is shown to include/encompass both storage areas 11a, 11b, 11c and internal registers 12a, 12b, and 12c, as shown in the citation above (Note that the drawing in Figure 5, included dashed lines does not exclude internal registers from address space shown on the left)]**.

(b) determining whether the non-volatile data storage has a single volume address space or a multiple volume address space based on the volume information;" **[With respect to this**

limitation, Suda discloses that "the memory card host device 1 includes a plural area authentication module 21 for judging whether or not a memory card subject to exchanging information has plural storage areas therein" (Figure 1 and Page 2, paragraph 0027, lines 1-4)]

"(c) operating the memory card as the *single* volume when said determining (b) determines that *the single volume address space* is present on the memory card;" **[With respect to this limitation, Suda discloses "where a judgment is made that there is only a single storage area, then normal processing takes place" (Pages 2-3, paragraph 0033, lines 10-11) and explains "in a memory card host device which cannot perform the above-described processing, the memory card remains in the state as shown in Fig. 4A when the power supply is turned on. Accordingly, such a memory card host device handles the memory card as the memory card having only the first storage area 11a" (Page 4, Par. 0050); thereby, operating the memory card as having a single volume]**

"and (d) operating the memory card *by dividing the address space of the non-volatile data storage into* a plurality of volumes when said determining (b) determines that *the multiple volume address space is* present on the memory card, one of the plurality of volumes being the first volume." **[Suda discloses this limitation as when judgment determines that a plurality of storage areas exist, then "the memory card switches storage areas so as to refer to a desired storage area" (Page 3, paragraph 0034, lines 1-3) and explains that "when the area has changed normally," then "data processing of the memory card by the memory card host device is performed" (Page 3, paragraph 0035, lines 8-10); thereby, operating the memory card as having a plurality of volumes].**

Assuming (*for the sake of argument*) that Suda's internal registers were not included in the address space defined by the contiguous range of addresses 00000 through xFFFF, as argued by Applicant, it would be obvious to one of ordinary skill in the art to place internal registers within this range or anywhere within memory card 3, since it involves a simple relocation of parts and it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse,* 86 USPQ 70.

Suda does not disclose expressly "(c) operating the memory card **by accessing the entire address space of the non-volatile data storage** as the single volume when said determining (b) determines that the single volume address space is present on the memory card."

To further detail the claimed limitations of "(c) operating the memory card by accessing the entire address space of the non-volatile data storage as the single volume when said determining (b) determines that the single volume address space is present on the memory card;" and "and "and (d) operating the memory card by dividing the address space of the non-volatile data storage into a plurality of volumes when said determining (b) determines that the multiple volume address space is present on the memory card, one of the plurality of volumes being the first volume." Kim discloses **["Optionally, the main body 10 further comprises a mode selection switch 15a. Using the mode selection switch 15a, one mode is selected from a single mode and a separate mode. When the single mode is selected, the flash memory card 16a is combined with the flash memory 11a, and the combined memories of the flash memory card 16a and flash memory 11a are recognized as a single drive (*which comprises accessing the entire space of the non-volatile data storage as a single volume*). Alternatively, when the separate mode is selected, the flash memory card 16a is separated from the flash**

memory 11a, the flash memory card 16a and the flash memory 11a are respectively recognized as individual drives (*which comprises dividing the address space of the non-volatile data storage into a plurality of volumes when it is determined multiple volumes are present*). For example, in case the flash memory 11a of the main body 10 is set as a D drive by the host computer, when the single mode is selected, the flash memory card 16a is set as the same D drive, thereby extending the capacity of the D drive. On the other hand, at this time, when the separate mode is selected, the flash memory card 16a is set as another drive different from the D drive of the flash memory 11a, such as an E drive" (Page 3, Par. 0043-0044)].

Suda (US 2004/0123059) and Kim et al. (US 2004/0123059) are analogous art because they are from the same field of endeavor of memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the memory card as described by Suda and have and provided an extended flash card in which in single mode, both flash cards are seen as a single drive which comprises operating the memory card by accessing the entire address space of the non-volatile data storage and in separate mode, each flash card is seen as separate drives as taught by Kim; thereby corresponding to the claimed single volume and plurality of volumes.

The motivation for doing so would have been because Kim discloses **["it is an object of the present invention to provide a portable flash memory which is simply connected to a USB port of a host computer so as to record and erase data, thereby being easy to extend in its memory capacity... to provide a portable flash memory with extended memory capacity**

in which an extended flash memory and a main flash memory are recognized as a single drive or as individual drives" (Page 1, Pars. 0007-008)].

Therefore, it would have been obvious to combine Suda (US 2004/0123059) with Kim et al. (US 2004/0123059) for the benefit of creating a method for reading data from a memory card to obtain the invention as specified in claim 1.

6. As per **claim 2 and 21**, the combination of Suda and Kim discloses "A method as recited in claims 1 and 20," **[See rejection to claim 1 above and rejection to claim 20 bellow]** "wherein the memory card includes a switch that has a plurality of switch positions," **[With respect to this limitation, Suda discloses "a large-capacity memory card which is arranged to switch plural storage areas with the use of mechanical switches provided on a housing" (Page 5, paragraph 0068 and paragraph 0069 (*see bellow*))]** "and wherein said operating (d) includes at least: (d1) determining a switch position for the switch; and (d2) selectively enabling one of the plurality of volumes based on the switch position" **[Suda discloses this limitation as "It is possible to select any one of the storage areas 11a and 11b of the memory card 3 by use of the mechanical switches 16a and 16b provided on the housing of the memory card 3. For example, when the mechanical switches 16a and 16b are set to positions marked as "1", the controller 10 reflects the state of the switches to the first internal register 12a, thereby allowing a memory card host device to handle the first storage area 11a. Similarly, when the mechanical switches 16a and 16b are set to positions marked as "2", the controller 10 reflects the state of the switches to the internal register 12a, thereby allowing the memory card host device to handle the second storage area 11b. Although FIG. 7 schematically shows the single internal register 12a, it is acceptable if the memory card 3**

includes the plural internal registers 12a, 12b, 12c, and 12d for the respective plural storage areas as shown in FIG. 1. Alternatively, it is also acceptable that the memory card 3 includes the internal register 18 for the plural storage areas as shown in FIG. 3" (Page 5, paragraph 0069)]. See Kim **[(Page 3, Par. 0043-0044 and Figure 1 and related text)]**. Kim further discloses **[switch 15a (Page 3, Par. 0043-0044)]**.

7. As per **claims 3 and 4**, the combination of Suda and Kim discloses "A method as recited in claim 2," **[See rejection to claim 2 above]** "wherein the switch has at least a first position and a second position, and wherein said operating (d) further includes at least:" **[See rejection to claim 2 above]** "(d3) imposing an address offset when the switch is in the second position; wherein the address offset enables the memory card to provide more data storage capacity than available with a file system using 16-bit addressing" **[Suda discloses this concept as "it is possible to maintain compatibility with a conventional memory card host device by setting the storage area having the file system that can be controlled by the conventional memory card host device as the storage area accessible when the power supply is turned on. Regarding the other storage areas, it is possible to moderate limitations of the storage capacities by changing the file systems thereof into file systems adopting new methods" (Page 5, paragraph 0066). Suda also explains that the size of storage areas "does not exceed the marginal capacity which can be handled by using a single file system. For example, when the FAT 16 is used as the file system, the marginal capacity is equal to 2 gigabytes" (Page 2, paragraph 0028, lines 14-17) and that "a conventional command length can only express an address up to the second storage area 11b. However, with the use of the address**

expressed with blocks enables expression of a large-capacity address" (Figure 5 and Page 4, paragraph 0057, lines 17-20)].

8. As per **claim 5**, the combination of Suda and Kim discloses "A method as recited in claim 2, wherein the switch has at least a first position and a second position," **[See rejection to claim 2 above]** "wherein, when the switch position is in the first position and the memory card is operated by dividing the address space of the non-volatile data storage into the plurality of volumes, the first volume of the non-volatile data storage is accessed, and wherein, when the switch position is in the second position and the memory card is operated by dividing the address space of the non-volatile data storage into the plurality of volumes, a second volume of the non-volatile data storage is accessed" **[With respect to this limitation, Suda discloses that "It is possible to select any one of the storage areas 11a and 11b of the memory card 3 by use of the mechanical switches 16a and 16b provided on the housing of the memory card 3. For example, when the mechanical switches 16a and 16b are set to positions marked as "1", the controller 10 reflects the state of the switches to the first internal register 12a, thereby allowing a memory card host device to handle the first storage area 11a" (Page 5, paragraph 0069) as changing the position of a switch to select different memory regions]**. See Kim **[(Page 3, Par. 0043-0044 and Figure 1 and related text and rejection to claim 1 above)]**.

9. As per **claim 6**, the combination of Suda and Kim discloses "A method as recited in claim 5," **[See rejection to claim 5 above]** "wherein the memory card is formatted into either one of a single volume or a pair of volumes, the pair of volumes being the first volume and the second volume" **[With respect to this limitation, Suda discloses that "where a judgment is**

made that there is only a single storage area, then normal processing takes place" (Page 3, paragraph 0033, lines 10-11) as an instance when a memory card is manages as a single storage area. Suda also discloses that when judgment determines that a plurality of storage areas exist, then "the memory card switches storage areas so as to refer to a desired storage area" (Page 3, paragraph 0034, lines 1-3) and explains that "when the area has changed normally," then "data processing of the memory card by the memory card host device is performed" (Page 3, paragraph 0035, lines 8-10) as having a plurality of volumes]. See Kim **[(Page 3, Par. 0043-0044 and Figure and related text)]**. See Kim **[(Page 3, Par. 0043-0044 and Figure 1 and related text)]**.

10. As per **claims 7, 10, and 17**, the combination of Suda and Kim discloses "A method as recited in claims 6, 13 and 28," **[See rejection to claim 6 above and rejection to claims 13 and 28 bellow]** "wherein the total non-volatile data storage for the memory card is formatted into the first volume of X gigabytes as the single volume, or formatted into the first and second volumes of X/2 gigabytes each as the pair of volumes" **[Suda discloses this concept as a memory card that can have either a single storage area or a plurality of storage areas wherein "The size thereof does not exceed the marginal capacity which can be handled by a single file system. For example, when the FAT 16 is used as the file system, the marginal capacity is equal to 2 gigabytes. In this event, the marginal capacity of the entire memory card is equivalent to 8 gigabytes when the memory card includes four storage areas as shown in FIG. 1, and is 10 gigabytes when the memory card includes five storage areas or 12 gigabytes when the memory card includes six storage areas" (Page 2, paragraph 0028) as having different**

memory capacities, depending on the number of partitions/storage areas within a memory card]. See Kim **[(Page 3, Par. 0033, 0043-0044 and Figure 1 and related text)]**.

11. As per **claims 8 and 9**, the combination of Suda and Kim discloses "A method as recited in claim 1," **[See rejection to claim 1 above]** "wherein said method further comprises: (e) detecting activation of the memory card, and wherein said accessing (a), said determining (b), and said operating (c) or (d) are performed once said detecting (e) detects the activation of the memory card" wherein "the activation of the memory card occurs upon power-on of the memory card or upon insertion of the memory card into a host device" **[With respect to this limitation, Suda discloses "a memory card authentication system according to the first embodiment of the present invention includes a memory card host device 1, a memory card 3, and a bus 2 for transmitting and receiving data" (Page 2, paragraph 0026) and also discloses, "the memory card 3 as shown in fig. 4A is in a state where the power supply is turned on. In this event, it is possible to handle the first storage area 11a" (Page 4, paragraph 0049)]**. See Kim **[(Page 1, Par. 0006 and 0009 and Figure 1 and related text)]**.

12. As per **claims 11-12, and 15-16**, the combination of Suda and Kim discloses "A method as recited in claim 1, 13 and 30-31," **[See rejection to claim 1 above]** "*wherein* when said determining (b) determines that *the single volume address space* is present on the memory card, the first volume *has* a FAT-32 file format" and "*wherein* when said determining (b) determines that *the multiple volume address space is* present on the memory card, each of the multiple volumes having a FAT-16 file format" **[Suda teaches this limitation as "when a memory card host device applies a certain file system and the maximum capacity which the file system can handle is .alpha., then the first embodiment enables the memory card host device to**

handle a memory card having a total capacity larger than .alpha. by having a configuration with plural storage areas each having a capacity less than .alpha. inside the memory card enabling the handling of a total capacity larger than .alpha.." (Page 2, paragraph 0025) as teaching a memory that can adopt any type of file system present in a host device connected to the memory card. Suda also provides an example in which "FAT 16 is used as the file system" (Page 2, paragraph 0028)].

13. As per **claims 13-14, and 24**, Suda discloses "A memory card having a single memory array defined by a contiguous range of addresses capable of being configured as a single partition having a first size or as multiple partitions each having a second size," as **["the present invention relates to a memory card authentication system, a memory card host device, a memory card, a storage area switching method, and a storage area switching program, which are capable of switching plural storage areas" (Page 1, paragraph 0003); and also teaches that "the memory card host device 1 includes a plural are authentication module 21 for judging whether or not a memory card subject to exchanging information has plural storage areas therein" (Figure 1 and Page 2, paragraph 0027, lines 1-4) and explains that "it is possible to handle a storage capacity larger than the marginal capacity of the file system by means of providing plural storage areas" (Page 2, paragraph 0030, lines 1-4) address space within memory card 3 (See Figure 1) and (Figure 5)]]**

"said memory card comprising: non-volatile data storage that provides data storage having an address space, said address space being configured to include at least a first partition, the first partition including partition information that is stored in a range of addresses that is a proper subset of the contiguous range of addresses;" **[Suda discloses this concept as "Fig. 1 shows the**

conventional memory card, in which flags are added to conventional reserved areas" (Page 3, paragraph 0039, lines 1-2) wherein "information indicating the corresponding storage area number is added hereto" (Page 3, paragraph 0039, lines 12-13) and "information indicating the quantity of the storage areas is added hereto"(Page 3, paragraph 0039, lines 25-26)]. Furthermore, Suda discloses Applicant should note that as the "internal register 18" stores the number of areas inside a memory card, this number of areas corresponds to the claimed "volume information." The number of areas inside a memory card represents the number of volumes inside a memory card, and therefore, represents "volume information." Furthermore, Suda discloses **["*FIG. 1 shows the conventional memory card, in which flags are added to convention reserved areas. Each of the internal registers 12a, 12b, 12c, and 12d of the memory card 3 includes first to third bit string 20a, 20b, and 20c... The first bit string 20a equivalent to the first 23 bits of the internal register indicates a characteristic of the memory card... The second bit string 20b equivalent to the first 23 bits of the internal register indicates a characteristic of the memory card 3... The third bit string 20c equivalent to 4 bits subsequent to the second bit string is also a convention reserved area of the internal register... Information indicating the quantity of storage areas is added hereto... In the memory card 3, shown in FIG. 1, a flag indicating 4 is et to each of the third bit strings of the internal register... when the memory card 3 has four storage areas*" (Par. 0039; See Figure 1 and related text)]**. Applicant should note that Examiner interprets the "first storage areas 11a-12a, 11b-12b, 11c-12c and 11d-12d" as a continuous address space which is shown as bit strings comprising fields 20a, 20b and 20c. Therefore, as Suda stores volume information indicating the number of storage areas within field 20c of internal registers, which are shown to comprise a

range of address that is a "proper subset" (*which comprises a relative term, as any subset within a storage address space can be considered a proper subset*) of a contiguous range of addresses, Suda discloses "accessing volume information stored in a *range of addresses that is a proper subset of the contiguous range of addresses that defines the address space*." Applicant should further note that Suda expressly discloses **["FIG. 5 shows the memory card 3 in which the plural storage areas 11a, 11b, and 11c severally include the internal registers 12a, 12b, and 12c" (Figure 5 and related text) wherein contiguous address space comprising addresses 00000-xFFFF is shown to include/encompass both storage areas 11a, 11b, 11c and internal registers 12a, 12b, and 12c, as shown in the citation above (Note that the drawing in Figure 5, included dashed lines does not exclude internal registers from address space shown on the left)]**.

"a switch being set in one of a plurality of switch positions;" **[With respect to this limitation, Suda discloses "a large-capacity memory card which is arranged to switch plural storage areas with the use of mechanical switches provided on a housing" (Page 5, paragraph 0068, lines 2-3)]**

"and a controller that manages access to the data stored in said non-volatile data storage," **[Suda discloses this limitation as "the controller 10 receives a command and data from the memory card host device 1 through the bus 2, and controls the storage areas based on the command and the data to the memory card" (Page 2, paragraph 0028, lines 6-9)]**

"wherein said controller is configured to examine the partition information stored in said first partition to determine whether the single partition or the multiple partitions are being used based on the partition information," **[With respect to this limitation, Suda discloses having**

"information indicating the quantity of storage areas" (Page 3, paragraph 0039, lines 25-26) and explains that "the memory card host device 1 refers to the reserved areas in accordance with the response from the controller 10 and interprets the flags" (Page 3, paragraph 0040, lines 10-13) which indicate the amount of storage areas being used]

"wherein when said controller determines that the single partition is used, said non-volatile data storage is accessed as a single partition, the first partition being the single partition," **[With respect to this limitation, Suda discloses "where a judgment is made that there is only a single storage area, then normal processing takes place" (Pages 2-3, paragraph 0033, lines 10-11) and explains "in a memory card host device which cannot perform the above-described processing, the memory card remains in the state as shown in Fig. 4A when the power supply is turned on. Accordingly, such a memory card host device handles the memory card as the memory card having only the first storage area 11a" (Page 4, Par. 0050); thereby, operating the memory card as having a single volume]**

"and wherein when said controller determines that the multiple partitions are being used, the address space of said non-volatile data storage is divided into multiple partitions, one of the multiple partitions being accessed based on the switch position of said switch" **[Suda discloses this limitation as when judgment determines that a plurality of storage areas exist, then "the memory card switches storage areas so as to refer to a desired storage area" (Page 3, paragraph 0034, lines 1-3) and explains that "when the area has changed normally," then "data processing of the memory card by the memory card host device is performed" (Page 3, paragraph 0035, lines 8-10). Suda also discloses "mechanical switches 16a and 16b for**

selecting one of the plural storage areas, and a controller 10 for reflecting the storage area selected by the mechanical switches" (Page 5, paragraph 0069, lines 1-4)].

Assuming (*for the sake of argument*) that Suda's internal registers were not included in the address space defined by the contiguous range of addresses 00000 through xFFFF, as argued by Applicant, it would be obvious to one of ordinary skill in the art to place internal registers within this range or anywhere within memory card 3, since it involves a simple relocation of parts and it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse,* 86 USPQ 70.

Suda does not disclose expressly "wherein when said controller determines that the single partition is used, the entire address space of said non-volatile data storage is accessed as a single partition, the first partition being the single partition."

To further detail the claimed limitations of "wherein when said controller determines that the single partition is used, the entire address space of said non-volatile data storage is accessed as a single partition, the first partition being the single partition," and "and wherein when said controller determines that the multiple partitions are being used, the address space of said non-volatile data storage is divided into multiple partitions, one of the multiple partitions being accessed based on the switch position of said switch," Kim discloses **["Optionally, the main body 10 further comprises a mode selection switch 15a. Using the mode selection switch 15a, one mode is selected from a single mode and a separate mode. When the single mode is selected, the flash memory card 16a is combined with the flash memory 11a, and the combined memories of the flash memory card 16a and flash memory 11a are recognized as a single drive (*which comprises accessing the entire address space of said non-volatile storage*

***as a single partition*). Alternatively, when the separate mode is selected, the flash memory card 16a is separated from the flash memory 11a, the flash memory card 16a and the flash memory 11a are respectively recognized as individual drives (*which comprises dividing address space of said non-volatile storage into multiple partitions*). For example, in case the flash memory 11a of the main body 10 is set as a D drive by the host computer, when the single mode is selected, the flash memory card 16a is set as the same D drive, thereby extending the capacity of the D drive. On the other hand, at this time, when the separate mode is selected, the flash memory card 16a is set as another drive different from the D drive of the flash memory 11a, such as an E drive" (Page 3, Par. 0043-0044)]**.

Suda (US 2004/0123059) and Kim et al. (US 2004/0123059) are analogous art because they are from the same field of endeavor of memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the memory card as described by Suda and have and provided an extended flash card in which in single mode, both flash cards are seen as a single drive wherein the entire address space of said non-volatile data storage is accessed as a single partition, the first partition being the single partition and in separate mode, each flash card is seen as separate drives as taught by Kim; thereby corresponding to the claimed single volume and plurality of volumes.

The motivation for doing so would have been because Kim discloses **["it is an object of the present invention to provide a portable flash memory which is simply connected to a USB port of a host computer so as to record and erase data, thereby being easy to extend in its memory capacity... to provide a portable flash memory with extended memory capacity**

in which an extended flash memory and a main flash memory are recognized as a single drive or as individual drives" (Page 1, Pars. 0007-008)].

Therefore, it would have been obvious to combine Suda (US 2004/0123059) with Kim et al. (US 2004/0123059) for the benefit of creating a method for reading data from a memory card to obtain the invention as specified in claims 13-14, and 24.

14. As per **claim 18, and 25**, the combination of Suda and Kim discloses "A memory card as recited in claim 13," **[See rejection to claim 13 above]** "wherein said memory card is a FLASH memory device" **[With respect to this limitation, Suda discloses that "the memory card 3 corresponds to a secure digital (SD) memory card" (Page 2, paragraph 0029, lines 1-2) wherein "a copyright protection function corresponding to the secure digital music initiative (SDMI) standard, and is upward compatible with a multimedia card (MMC). The SD memory card is a memory card based on the SDMI standard which has been jointly developed by three companies Toshiba Corporation, Matsushita Electric Industrial Co., Ltd., and SanDisk Corporation" (Page 2, paragraph 0029) and explains addressing the memory card in block units instead of byte units (Page 4, paragraph 0057), which is equivalent to having a flash memory card]**. Kim discloses flash memory 11 and flash memory 21 **[(Figure 1 and related text)]**.

15. As per **claim 19-20, and 22-23**, the combination of Suda and Kim discloses the limitations required by claims 19-20, and 22-23 which rejected for the same reasons as recited above for claim 13; further requiring:

"means for accessing volume information stored in a range of addresses that is a proper subset of the contiguous range of addresses that defines the address space;" ***(page 3, paragraph 0012,***

lines 7-8 and page 9, paragraph 0043, lines of applicant's specification identifies this means as "controller 402") **[With respect to this limitation, Suda discloses "the controller 10 receives a command and data from the memory card host device 1 through the bus 2, and controls the storage areas based on the command and the data to the memory card" (Page 2, paragraph 0028, lines 6-9) and that "information indicating the quantity of storage areas" (Page 3, paragraph 0039, lines 25-26) and explains that "the memory card host device 1 refers to the reserved areas in accordance with the response from the controller 10 and interprets the flags" (Page 3, paragraph 0040, lines 10-13) which indicate the amount of storage areas being used"]** Applicant should note that as the "internal register 18" stores the number of areas inside a memory card, this number of areas corresponds to the claimed "volume information." The number of areas inside a memory card represents the number of volumes inside a memory card, and therefore, represents "volume information." Furthermore, Suda discloses [***"FIG. 1 shows the conventional memory card, in which flags are added to convention reserved areas. Each of the internal registers 12a, 12b, 12c, and 12d of the memory card 3 includes first to third bit string 20a, 20b, and 20c... The first bit string 20a equivalent to the first 23 bits of the internal register indicates a characteristic of the memory card... The second bit string 20b equivalent to the first 23 bits of the internal register indicates a characteristic of the memory card 3... The third bit string 20c equivalent to 4 bits subsequent to the second bit string is also a convention reserved area of the internal register... Information indicating the quantity of storage areas is added hereto... In the memory card 3, shown in FIG. 1, a flag indicating 4 is et to each of the third bit strings of the internal register... when the memory card 3 has four storage areas***" **(Par. 0039; See Figure 1 and**

related text)]. Applicant should note that Examiner interprets the "first storage areas 11a-12a, 11b-12b, 11c-12c and 11d-12d" as a continuous address space which is shown as bit strings comprising fields 20a, 20b and 20c. Therefore, as Suda stores volume information indicating the number of storage areas within field 20c of internal registers, which are shown to comprise a range of address that is a "proper subset" (*which comprises a relative term, as any subset within a storage address space can be considered a proper subset*) of a contiguous range of addresses, Suda discloses "accessing volume information stored in a *range of addresses that is a proper subset of the contiguous range of addresses that defines the address space*." Applicant should further note that Suda expressly discloses **["FIG. 5 shows the memory card 3 in which the plural storage areas 11a, 11b, and 11c severally include the internal registers 12a, 12b, and 12c" (Figure 5 and related text) wherein contiguous address space comprising addresses 00000-xFFFF is shown to include/encompass both storage areas 11a, 11b, 11c and internal registers 12a, 12b, and 12c, as shown in the citation above (Note that the drawing in Figure 5, included dashed lines does not exclude internal registers from address space shown on the left)]**

"means for determining whether a single volume address space or a multiple volume address space is present on said memory device based on the volume information;" ***(page 3, paragraph 0012 and page 9, paragraph 0043, lines of applicant's specification identifies this means as "controller 402")*** **With respect to this limitation, Suda discloses "where a judgment is made that there is only a single storage area, then normal processing takes place" (Pages 2-3, paragraph 0033, lines 10-11)]**

"and means for operating said memory device based on a configuration of said memory device by accessing the entire address space of the non-volatile data storage as a single volume, or by dividing the address space of the non-volatile data storage into multiple volumes based on a determination of said means for determining" (***page 9, paragraph 0044, lines 4-6 defines this means as "memory controller 402"***) **[Suda discloses this limitation as when judgment determines that a plurality of storage areas exist, then "the memory card switches storage areas so as to refer to a desired storage area" (Page 3, paragraph 0034, lines 1-3) and explains that "when the area has changed normally," then "data processing of the memory card by the memory card host device is performed" (Page 3, paragraph 0035, lines 8-10). Suda also discloses "mechanical switches 16a and 16b for selecting one of the plural storage areas, and a controller 10 for reflecting the storage area selected by the mechanical switches" (Page 5, paragraph 0069, lines 1-4). Kim discloses mode selection switch and microcomputer 14a (Figure 2 and related text; Page 3, Par. 0043-0044)]**.

Assuming (*for the sake of argument*) that Suda's internal registers were not included in the address space defined by the contiguous range of addresses 00000 through xFFFF, as argued by Applicant, it would be obvious to one of ordinary skill in the art to place internal registers within this range or anywhere within memory card 3, since it involves a simple relocation of parts and it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse,* 86 USPQ 70.

ACKNOWLEDGMENT OF ISSUES RAISED BY THE APPLICANT

Response to Amendment

16. Applicant's arguments filed on October 24, 2007 with respect to claims **1-25** have been considered but are not persuasive.

17. As required by **M.P.E.P. § 707.07(f)**, a response to these arguments appears below.

ARGUMENTS CONCERNING PRIOR ART REJECTIONS

18. Claims must be given the broadest reasonable interpretation during examination and limitations appearing in the specification but not recited in the claim are not read into the claim (See M.P.E.P. 2111 [R-1]).

FIRST POINT OF ARGUMENT

19. Regarding Applicant's remark that Suda does not disclose "volume information stored in a range of addresses that is a proper subset of the contiguous range of addresses that defines the address space" as internal registers in Suda are not included in the address space defined by the contiguous range of addresses 00000 through xFFFF; the Examiner disagrees.

Applicant should note that Suda discloses "volume information stored in a range of addresses that is a proper subset of the contiguous range of addresses that defines the address space" as the "internal register 18" stores the number of areas inside a memory card, this number of areas corresponds to the claimed "volume information." The number of areas inside a memory card represents the number of volumes inside a memory card, and therefore, represents "volume information." Furthermore, Suda discloses [***"FIG. 1 shows the conventional memory card, in which flags are added to convention reserved areas. Each of the internal registers 12a, 12b,***

***12c, and 12d of the memory card 3 includes first to third bit string 20a, 20b, and 20c... The first bit string 20a equivalent to the first 23 bits of the internal register indicates a characteristic of the memory card... The second bit string 20b equivalent to the first 23 bits of the internal register indicates a characteristic of the memory card 3... The third bit string 20c equivalent to 4 bits subsequent to the second bit string is also a convention reserved area of the internal register... Information indicating the quantity of storage areas is added hereto... In the memory card 3, shown in FIG. 1, a flag indicating 4 is et to each of the third bit strings of the internal register... when the memory card 3 has four storage areas*" (Par. 0039; See Figure 1 and related text)]. Applicant should note that Examiner interprets the "first storage areas 11a-12a, 11b-12b, 11c-12c and 11d-12d" as a continuous address space which is shown as bit strings comprising fields 20a, 20b and 20c. Therefore, as Suda stores volume information indicating the number of storage areas within field 20c of internal registers, which are shown to comprise a range of address that is a "proper subset" (*which comprises a relative term, as any subset within a storage address space can be considered a proper subset*) of a contiguous range of addresses, Suda discloses "accessing volume information stored in a *range of addresses that is a proper subset of the contiguous range of addresses that defines the address space*." Applicant should further note that Suda expressly discloses **["FIG. 5 shows the memory card 3 in which the plural storage areas 11a, 11b, and 11c severally include the internal registers 12a, 12b, and 12c" (Figure 5 and related text) wherein contiguous address space comprising addresses 00000-xFFFF is shown to include/encompass both storage areas 11a, 11b, 11c and internal registers 12a, 12b, and 12c, as shown in the citation above (Note that the**

drawing in Figure 5, included dashed lines does not exclude internal registers from address space shown on the left)].

20. Assuming (*for the sake of argument*) that Suda's internal registers were not included in the address space defined by the contiguous range of addresses 00000 through xFFFF, as argued by Applicant, it would be obvious to one of ordinary skill in the art to place internal registers within this range or anywhere within memory card 3, since it involves a simple relocation of parts and it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse,* 86 USPQ 70.

21. All arguments by the applicant are believed to be covered in the body of the office action; thus, this action constitutes a complete response to the issues raised in the remarks dated October 24, 2007.

CLOSING COMMENTS

Examiner's Note

22. Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant, in preparing the responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner.

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

23. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

24. Per the instant office action, claims 1-25 have received a first action on the merits and are subject of a non-final rejection.

b. DIRECTION OF FUTURE CORRESPONDENCES

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yaima Campos whose telephone number is (571) 272-1232. The examiner can normally be reached on Monday to Friday 8:30 AM to 5:00 PM.

IMPORTANT NOTE

26. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Sanjiv Shah, can be reached at the following telephone number: Area Code (571) 272-4098.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more

information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

December 19, 2007

Yaima Campos
Examiner
Art Unit 2185

SANJIV SHAH
SUPERVISORY PATENT EXAMINER
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